REMARKS

Claims 1-5 and 7-25 are currently active.

Claim 6 has been canceled with its limitations added to Claim 1.

Claim 25 has been added. Antecedent support for Claim 25 is found on page 13, lines 5 and 6.

Antecedent support for the amendments to the claims is found on page 15, lines 5-19 and Claim 13.

The Examiner has rejected Claims 1, 2, 15, 16 and 18-21 as being anticipated by Tout. Applicant respectfully traverses this rejection.

Referring to Tout, there is disclosed a digital switch. Tout teaches that data is received and transmitted securely over either fiber twisted pair cables connected to the switch ports 3. At the interface between the port cards 2 and the switch fabric card 5 the data is 8-bit parallel with a single bit start of cell signal. An ATM cell passing from the port card 2 to the switch fabric card 5 is prepended with a 3-byte internal routing tag which is generated using a

look-up algorithm from the contents of the address field and the ATM header. The prepended routing tag comprises 2 bits defining the service class and a further 18 bits identify one or more destination ports. The remaining 4 bits are reserved. The internal routing tag is removed when the cell is prepared for transmission from the appropriate port card 2. See column 6, line 61-column 7, line 6.

Tout teaches the switch fabric card 5 comprises a switch fabric data controller ASIC 6 connected to 4 traffic control ASICs 7 and a shared memory 8. The switch fabric card 5 uses a shared memory 8 to provide a large buffering of ATM cells. This becomes necessary when the total input port bandwidth transmitted to any given output port exceeds the output bandwidth of 155.52 Mbps. Each of the traffic control ASICs 7 has the function of concentrating 5 full-duplex switch fabric ports 9 at 155 Mbps each into a single full-duplex 800 Mbps stream. This stream is carried on an 8-bit data bus 10 with control signals which delivers the 56-byte ATM cells to the switch fabric controller ASIC 6 in quarter cell segments, i.e. 14-bytes. This allows each switch fabric port 9 to pass data to the switch fabric at a controller ASIC 6 without having to wait for complete cells. This gives a more balanced latency and contributes to the overall low latency of the ATM switch. The data stream from each of traffic control ASIC 7 to the switch fabric data control ASIC 6 is a time division multiplexing TDM stream of 5 repeating slots each marked by an active high strobe signal. Each slot has an interval of 14 100 MHz cycles with the strobe signal active during the first

cycle of each slot. A complete quarter cell segment from the switch fabric port 9 can be transmitted in one such slot. There is no fixed mapping between the 5 switch fabric ports 9 and the 5 repeating slots. The first quarter cell segment to arrive from the switch fabric port will be transmitted and the next available slot will reserve that slot for all four segments of the cell using flags. The slot will only be released for re-allocation if a non-continuous stream of ATM cells is being received at that port. See column 7, lines 10-42.

Claim 1 has the limitation of "said providing mechanism transferring more than one packet at a time in the allocated time slot whose total width equals the width of the carrier mechanism in each allocated time slot to the memory mechanism, said providing mechanism transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet from an input stage queue group to fill the width but not transferring any data from any packets from the input stage queue group in the allocated time slot when there is not enough data to fill the total width of the carrier mechanism". This is distinct from the prior art, such as Tout, where due to packet fragmentation on the memory bus, typical TDM switching systems utilized bus widths that are at most as wide as a minimum length packet. See page 3, lines 3-11 of the above-identified patent application.

To reiterate, Tout is the typical prior art system that has narrowed down the memory bus bandwidth to be less than the bandwidth of the incoming ports to minimize or eliminate packet fragmentation. Another way of saying this is that by Tout teaching to transfer a quarter cell segment in each cycle, there will generally always be bites of data to fill the 8-bit data bus 10. This is exactly the opposite of the invention of Claim 1 of applicant. In applicant's invention of Claim 1, applicant accumulates data so that more data can be transmitted along the carrier mechanism each cycle than is received by a port at the cycle and only if there is enough data to fill the width. If there is not enough data to fill the width, the time slot is allowed to pass by, but the data is not provided to the time slot. Tout does not teach or suggest anything like this, and in fact teaches the opposite, and thus away from applicant's invention of Claim 1 by limiting the transfer of data on the bus to a quarter of a cell segment, which is less than the input port's bandwidth, in every transfer cycle.

It appears that Tout does not even teach the limitation of "transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet to fill the total width but not transferring any data from any packets in the allocated time slot when there is not enough data to fill the total width of the carrier mechanism". All that Tout teaches is to transfer quarter cell segments in each slot. Tout teaches that on an 8-bit data bus 10 is delivered the 56-byte ATM cells to the switch fabric controller ASIC 6 in quarter cell segments, i.e. 14-bytes. There is nothing that

indicates that 14-bytes equals the width of the 8-bit data bus. It is respectfully submitted that the Examiner must take the teachings of Tout in the context they are found, and not read limitations of applicant's claimed invention into the teachings of Tout, where they are not there. A straightforward and careful reading of Tout simply shows that an ATM cell is transferred from a fabric port 9 along an 8-bit data bus in quarter cell segments where each segment is provided in a slot of a time division multiplexing, with the first quarter cell segment reserving that slot for all four segments of the cell using flags. See column 7, lines 17-42.

The Examiner states in the Office Action that this language of applicant's claimed invention is met by the teachings of figure 5 and figure 2, reference 6 which is a controller for providing the packets to the memory in each transfer cycle where the bus between the input port and memory has a width which is equal to a portion of the packet; and the width of carrier mechanism is met by figure 2 reference 10 and has a width 8 bit and input and port mechanism is serial, is wider than the width of the input and output port mechanism. Respectfully, applicant cannot find any such language stated in Tout that supports the Examiner's position. Applicant has carefully discussed the text, in relevant part, of Tout and has not found the language that the Examiner has relied on for the rejection. To reiterate, no where can applicant find any language in Tout, that teaches or states as the Examiner suggests, that the bus between the input port and memory has a width which is equal to a portion of the

packet, let alone the other limitations mentioned above. Applicant respectfully requests the Examiner to specifically state by column and line number the text that shows the specific relationship. Applicant submits that Tout is totally quiet about the equal relationship of the bus width and the portion of the packet; on the contrary, Tout teaches that the bus width is larger than the portion of the packet that is being transferred in each cycle, thus there is packet fragmentation in Tout. Accordingly, Tout does not anticipate Claim 1.

Applicant notes that there is the statement in column 7, lines 18-20 that each of the traffic control ASICs 7 has the function of concentrating 5 full-duplex switch fabric ports 9 at 155 Mbps each into a single full-duplex 800 Mbps stream. This concentration takes place in the ASIC 7 and has nothing to do what happens in regard to the bus to the memory from the ASIC 7.

Claim 2 is dependent to parent Claim 1 and is patentable for the reasons Claim 1 is patentable. Moreover, Claim 2 has the limitation that the width of the carrier mechanism is independent of the width of the packet. Tout specifically requires the width of the data bus 10 be a function of the quarter segment of a cell. For this reason, Claim 2 is also patentable.

Claim 15 is patentable for the reasons similar to Claim 1. Claim 15 does not have packet fragmentation or any limitation on the effective bandwidth of the input port

mechanism and output port mechanism, and a central resource having a width which is independent of any input or output port mechanisms' width. The applied art of record has a distinct limitation on the data bus 10 in regard to the requirement that it can only transfer quarter cell segments in a slot. For this reason, Claim 15 is patentable over Tout. Claim 16 is dependent to parent Claim 15 and is patentable for the reasons Claim 15 is patentable.

Claim 18 has the limitation of "a mechanism for reading and writing data of packets to the memory mechanism through the bus without knowledge of the packet boundaries of the data". As explained above, Tout specifically requires knowledge of the packet boundaries because Tout requires quarter cell segments to be transferred in the slots during time division multiplexing. The only way that Tout can know about, or form the quarter cell segments, is to know the packet boundaries of the data. Accordingly, for this reason, Claim 18 is patentable. Claim 18 is essentially also patentable for the reasons Claim 1 is patentable.

Claim 19 has the limitation of "an input stage mechanism having a width for providing data of packets to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple > 1 of the input stage mechanism width". As explained above, the data bus 10 has a width which

is no more than a multiple of one, and is actually taught to be less than one of the width of the input port taught by Tout. For this reason, Claim 19 is patentable over Tout.

In regard to Claim 20, there is the limitation that "said bus width not a function of the data contained in a packet". As explained above, Tout teaches that the bus 10 width is a fixed function equal to a quarter segment of a cell. For this reason, Claim 20 is patentable over Tout.

Claim 21 is dependent to parent Claim 20 and is patentable for the reason Claim 20 is patentable. Moreover, Claim 21 has the limitation that the bus width is a positive non-integer multiple of the packet size greater than one. For the reasons Claim 19 is patentable over Tout, Claim 21 is also patentable over Tout.

The Examiner has rejected Claims 3-12, 14, 17 and 22 as being patentable over Tout and further in view of Fukano. Applicant respectfully traverses this rejection.

In regard to Claims 3 and 4, the Examiner takes official notice regarding the transmission and reception of a variable size packets being well known in the arch at the time of the invention. The applicant notes that Claims 3 and 4 are dependent to parent Claim 1 and

have all the limitations of parent Claim 1. For the reasons Claim 1 is patentable over Tout, Claims 3 and 4 are also patentable over Tout.

In regard to Claim 5, there is the limitation that the providing mechanism also provides packets from the memory mechanism to the output port mechanism through the carrier mechanism, said providing mechanism able to transfer packets or portions of packets whose total data equals the width of the carrier mechanism in each transfer cycle from the memory mechanism. Tout does not teach or suggest this limitation. Tout teaches the switch fabric data controller ASIC 6 returns the 56-byte ATM cells to the traffic control ASIC 7 using the 800 Mbps stream in eighth cell segments, i.e. seven-bytes. This allows the traffic control ASIC 7 to start transmitting data from the switch fabric data controller ASIC 6 back to the desired switch ports 3 on the port card 2 without the need for the switch fabric data controller ASIC 6 to be in possession of a complete cell Lahore. See column 7, lines 42-50. There is no teaching that the eighth cell segments are equal in width to the width of the bus on which they travel. Again, Tout is silent regarding this limitation. Accordingly, Claim 5 is patentable over Tout, in addition to the reasons that Claim 5 is dependent to parent Claim 1 and is patentable for the reasons Claim 1 is patentable.

Referring to Fukano, there is disclosed an input/output buffer type ATM switch. Fukano teaches the cells stored in each of the queues in input buffers are inputted and

sequenced into the inner bus 14 through the access control part 12 for each of the output ports, and outputted to the predetermined address port. The queue of the CBR has a higher priority than another queue of the ABR for the same output port in the same input buffer. Therefore, as far as a cell is stored in the queue of the CBR, the cell is always outputted from the queue of the CBR, and the cell in the queue of lower priority is outputted only in the case where no cell exists in the queue of the CBR. See column 6, lines 20-30.

The inner bus 14 is a time sharing bus, that has a data transmission rate of n-times of that of each of the input ports, so that it is guaranteed that the cells can be transmitted from each of the input ports one by one within a one cell period. See column 6, lines 35-40. The receiving buffers are arranged for each of the output ports with each of the receiving buffers being memory operated at the data transmission rate of the inner bus and the memory capacities generally being quite low as compared with those of the output buffers. See column 6, lines 42-47.

Two threshold values, the second threshold value A and the first threshold value B are provided in each of the idle queues, and at the time when the length of the idle queue becomes short and is reached to the first threshold value B, the first RNR signals are generated. The first RNR signals generated from each of the output buffers are multiplexed by

the multiplex circuit so as to produce the third RNR signal and this signal is inputted to each of the input buffers. See column 6, line 60-column 7, line 2.

The third RNR signal contains a discriminating number of the output buffers generating the first RNR signal, each of the input buffers receiving the third RNR signal stops the cell output from the low priority queue of ABR corresponding to the output buffer generating the first RNR signal until disappearing the first RNR signal from the output buffer. See column 7, lines 4-9.

Fukano teaches the second threshold value A is set to a lower value than the first threshold value, and when the length of the idle queue becomes shorter and reaches the second threshold value A, the second RNR signals are generated and inputted to each of the receiving buffers respectively corresponding to the output buffer generating the second RNR signal. See column 7, lines 14-21. The second threshold value date is set such that the remaining capacity of the output buffer is scarcely present, and so the receiving buffer which has received the second RNR signal stops the cell output to the corresponding output buffer. At this time, cell transmission of any priority is stopped. See column 7, lines 22-26.

The receiving buffers are also provided with each threshold value to control cell transmission, and when the cell amount stored in each of the receiving buffers exceeds this

threshold value, the fourth RNR signal is generated and inputted to the multiplex circuit. The multiplex circuit generates a fifth RNR signal including a discriminating number of the output buffer corresponding to the receiving buffer generating the fourth RNR signal in the same manner as that of the first RNR signal and the third RNR signal, and inputs it in each of the input buffers. Each of the input buffers stops outputting of cells for the output port corresponding to the output port buffer indicated in the fifth RNR signal being received. See column 7, lines 28-40.

In regard to Claim 1, there is no teaching or suggestion of "transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet to fill the total width but not transferring any data from any packets in the allocated time slot when there is not enough data to fill the total width of the carrier mechanism," as found in Claim 1. All that Fukano teaches is that the inner bus 14 is a time sharing bus that has a data transmission rate of n-times of that of each of the input ports, so that it is guaranteed that the cells can be transmitted from each of the input ports one by one within a one cell period. See column 6, lines 35-41. Accordingly, Fukano does not add anything to the teachings of Tout, in relevant part, in regard to the limitations of Claim 1 to arrive at Claim 1. Claims 3-12 and 14 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

Fukano does not add anything to the teachings of Tout in regard to the limitation of Claims 2-6 either, and these claims are also independently patentable over Tout in view of Fukano for this reason also.

Additionally, the Examiner has taken the position that because Tout fails to disclose the claimed invention regarding Claims 6-9 and the limitation of the stage queue groups and output stage queue groups, Fukano provides these teachings, and Fukano in combination with Tout arrive at the limitations of Claims 6-9. Applicant respectfully traverses this position of the Examiner. The teachings of Tout and Fukano are not compatible and cannot be combined. As is well known patent law, the Examiner cannot combine teachings of references out of the context in which they are found. As explained above, there are so many differences in the operation of these two references, that applicant has no clue how they would be combined without a significant redesign and development of either of the systems of their respective references to make an operable system. Tout instead teaches to transfer quarter cell segments on the data bus 10 to the switch fabric controller ASIC 6. The transfer amount is fundamental to each respective system taught in Tout or Fukano. Furthermore, in order for the receiving buffers and output buffers taught by Fukano to be used, two threshold values need to be identified and three different RNR signals need to be created. There is no explanation, let alone teaching or suggestion how one skilled in the art would combine or apply these threshold values or RNR signals to the teachings of Tout, where there are no such

input and output buffers, let alone threshold values or RNR signals. The abstinence of these factors in the teachings of Tout indicate that not only are they not necessary, Tout teaches away from their use. The focus of Tout is in regard to the manipulation of these quarter cell segments and applicant is at a loss where the buffers taught by Fukano would be introduced into the architecture of Tout and utilized in the way that they are taught, thus the context by Fukano. There must be some teaching or suggestion in the references of Tout and Fukano to combine these teachings, and there is none, let alone how they would be introduced.

Moreover, the Examiner is using the hindsight from applicant's own claims as a road map to find the various limitations of the claims in the prior art, and by having found each of the elements, concludes that the claims are arrived at. This also is contrary to patent law. There is no reason why one skilled in the art would modify the architecture of Tout to include the buffers and how the buffers are used with all their features of Fukano, into Tout, because Tout has no need for them. Accordingly, for these reasons also, Claims 3-12 and 14 are patentable over Tout in view of Fukano.

In regard to Claim 17, it is dependent to parent Claim 15 and is patentable for the reasons Claim 15 is patentable. Claim 15 is patentable over Tout in view of Fukano for the reasons Claim 1 is patentable over Tout in view of Fukano. Claim 17 is also patentable for the reasons explained above in regard to Claim 6.

Claim 22 is patentable for the reasons Claim 20 is patentable over Tout in view of Fukano, since Claim 22 is dependent from Claim 20. Claim 20 is patentable over Tout in view of Fukano for the reasons Claim 2 is patentable over Tout in view of Fukano.

The Examiner has rejected Claims 13 and 23-24 as being on patentable over Tout in view of Fukano and Lyons. Applicant respectfully traverses this rejection.

Referring to Lyons, there is disclosed a method and apparatus for operating a transport stream encoder to produce a stream of packets caring data representing a plurality of components signals. Lyons teaches that there are produced a plurality of digital signal components, respectively coupled to a corresponding plurality of the input terminals 5. The plurality of the input terminals 5 are respectively coupled to data input terminals of a corresponding plurality of FIFO buffers 10. Respective data output terminals of the FIFO buffers are coupled in common to a data bus 20. The data bus 20 is also coupled to a data input terminal of a packetizer 30. An output terminal of the packetizer 30 is coupled to an output terminal 15. The output terminal 15 is coupled to the transport links for processing the packet stream and broadcasting it to remote locations. A scheduler controller 50 includes a ready signal input terminal and identifier signal and enable signal output terminals. The respective ready output terminals of each of the plurality of FIFO buffers are coupled in common to the ready input terminal of the scheduler controller 50. The identifier of port

terminal ID of the scheduler controller 50 is coupled common to respective identifier input terminals ID of each of the plurality of FIFO buffers 10, and the enable output terminal E of the scheduler controller 50 is coupled in common to the respective enable input terminals of each of the plurality of FIFO buffers 10. The signal lines coupling together the ready, identifier ID and enable terminals form a control bus 22, which operates in conjunction with the data bus 20. A start signal output terminal of the packetizer 30 is coupled to a start signal input terminal of the scheduler controller 50. A memory 70 is coupled to the scheduler controller 50. A user input terminal 25 which is coupled to the source of user input is coupled to an input port of a microprocessor 60. The microprocessor has a control output port coupled to a control input terminal of the scheduler controller 50. The operation of the packetizer 30 produces a stream of sequential packets. Each packet contains data from one of the components signals, or, if there is not enough data in that component FIFO at the time the packet is formed, a null packet. The packet stream is divided into successive groups of packet slots, each group having a predetermined number of packets slots. The scheduler controller 50 controls which signal component is inserted into each packet slot. The scheduler controller 50 contains a set of lists of permissible signal components, one list for each packet slot. The set of lists are stored in the memory associated with the scheduler controller 50. If the scheduler controller 50 is operated as an input output adapter of the microprocessor, then a set of lists is stored in the one in the microprocessor, otherwise, the scheduler controller 50 contains its own memory to contain the set of lists. Each FIFO buffer 10 has a predetermined

unique address or identification value associated with it, and the scheduler controller 50 maintains an identification value of each FIFO buffer 10 in its list. When it is time to fill a packet slot, the list of permissible signal components for the packet slot is traversed. The scheduler controller 50 places an identification signal containing the predetermined unique identification value for the first signal components FIFO buffer 10 on the ID signal line.

As can be seen from the above description, there is no teaching or suggestion of the limitation of "transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet to fill the total width but not transferring any data from any packets in the allocated time slot when there is not enough data to fill the total width of the carrier mechanism," as found in Claim 1. In fact, Lyons is completely silent in regard to this limitation. Lyons adds nothing to the teachings of Tout or Fukano to arrive at the limitations of Claim 1. Accordingly, Claim 1 is patentable over Tout in view of Fukano and Lyons. Claim 13 is dependent to parent Claim 1 and is patentable for the reasons Claim 1 is patentable over Tout in view of Fukano or Lyons.

Similarly, Claim 20 is patentable over Tout in view of Fukano and Lyons for the reasons Claim 2 is patentable over Tout in view of Fukano, as explained above, and further in combination with Lyons, since Lyons also adds nothing to the teachings of Tout and Fukano in regard to the limitations of Claim 20. Claims 23 and 24 are dependent to parent

Claim 20 and are patentable for the reasons Claim 20 is patentable over Tout in view of Fukano than Lyons.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-5 and 7-25, now in this application be allowed.

Respectfully submitted,

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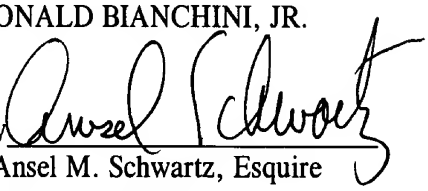
By 

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Version with markings to show changes made to the claims

1. A switching system comprising:

I input port mechanisms with a width, which receive packets having data from a communication line, where I is greater than or equal to 1 and is an integer;

O output port mechanisms with a width, which send packets to a communication line, where O is greater than or equal to 1 and is an integer;

a carrier mechanism for carrying packets in an allocated time slot, said carrier mechanism having a width wider than the width of the input and output port mechanisms so data from more than one packet at a time is transferred in the allocated time slot, said carrier mechanism connected to each input port mechanism and each output port mechanism;

a memory mechanism in which packets are stored, said memory mechanism connected to the carrier mechanism; and

a mechanism for providing [packets] data from more than one packet at a time to the memory mechanism through the carrier mechanism from the input port mechanisms, the providing mechanism includes input stage queue groups connected to the carrier mechanism

and the input port mechanisms for storing packets received by the input port mechanisms, and output stage queue groups connected to the providing mechanism and the output port mechanisms for storing packets to be sent out the output port mechanisms, said providing mechanism [able to transfer packets or portions of packets] transferring more than one packet at a time in the allocated time slot whose total width equals the width of the carrier mechanism in each [transfer cycle] allocated time slot to the memory mechanism, said providing mechanism transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet from an input stage queue group to fill the width but not transferring any data from any packets from the input stage queue group in the allocated time slot when there is not enough data to fill the width of the carrier mechanism.

7. A system as described in Claim [6] 5 wherein the providing mechanism includes a classifying mechanism which places a packet which is received by the input port mechanism into a corresponding queue group, said classifying mechanism connected to the input port mechanisms and the input stage queue groups.

15. A switching system for packets comprising:

a central resource having a width and an overall bandwidth and input port mechanisms and output port mechanisms each having widths for receiving or sending packets, respectively, said central resource partitioned via time slots that are allocated to the input and output port mechanisms, said central resource width independent of any input or output port mechanisms width and the overall bandwidth can grow without limitation by the input or output port mechanisms width; and

a memory mechanism for storing packets, said memory mechanism connected to the central resource and receiving more than one packet at a time in a respective time slot from the central resource which completely fills the width of the central resource, the central resource transferring more than one packet at a time to the memory mechanism in the respective time slot only when there is enough data from more than one packet to fill the total width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the total width of the carrier mechanism.

18. A switching system comprising:

a time division multiplex bus having a width;

a memory mechanism connected to the bus which is accessed via time slots in time division multiplexing of the bus; and

a mechanism for reading and writing data of packets to the memory mechanism through the bus without knowledge of the packet boundaries of the data, the reading and writing mechanism transferring more than one packet at a time to or from the memory mechanism in a respective time slot only when there is enough data from more than one packet to fill the width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the width of the bus.

19. A switching system comprising:

a time division multiplex carrier mechanism having a width;

a memory mechanism connected to the carrier mechanism which is accessed via time slots in time division multiplexing of the bus; and

an input stage mechanism having a width for providing data of packets to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple of the input stage mechanism

width a mechanism for providing data of packets having a width to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple of the packet width greater than one, the input stage mechanism transferring more than one packet at a time to the memory mechanism in a respective time slot only when there is enough data from more than one packet to fill the width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the width of the carrier mechanism.

20. A method for switching packets having a width comprising the steps of:

receiving a first packet and at least a second packet at a switch mechanism; and

transferring data of the first packet and the second packet to a memory mechanism via time slots in time division multiplexing of a bus having a width [so] only when data from the packets fills a predetermined portion of the width of the bus in a time slot, but not transferring any data from the first and second packets in the time slot when there is not enough data to fill the predetermined portion of the width of the bus, said bus width not [necessarily] a function of the data contained in any packet.